Context Update of Aquila Interoperability Package (Aquila Lite) - Control Architecture and Philosophies

13th June 2024

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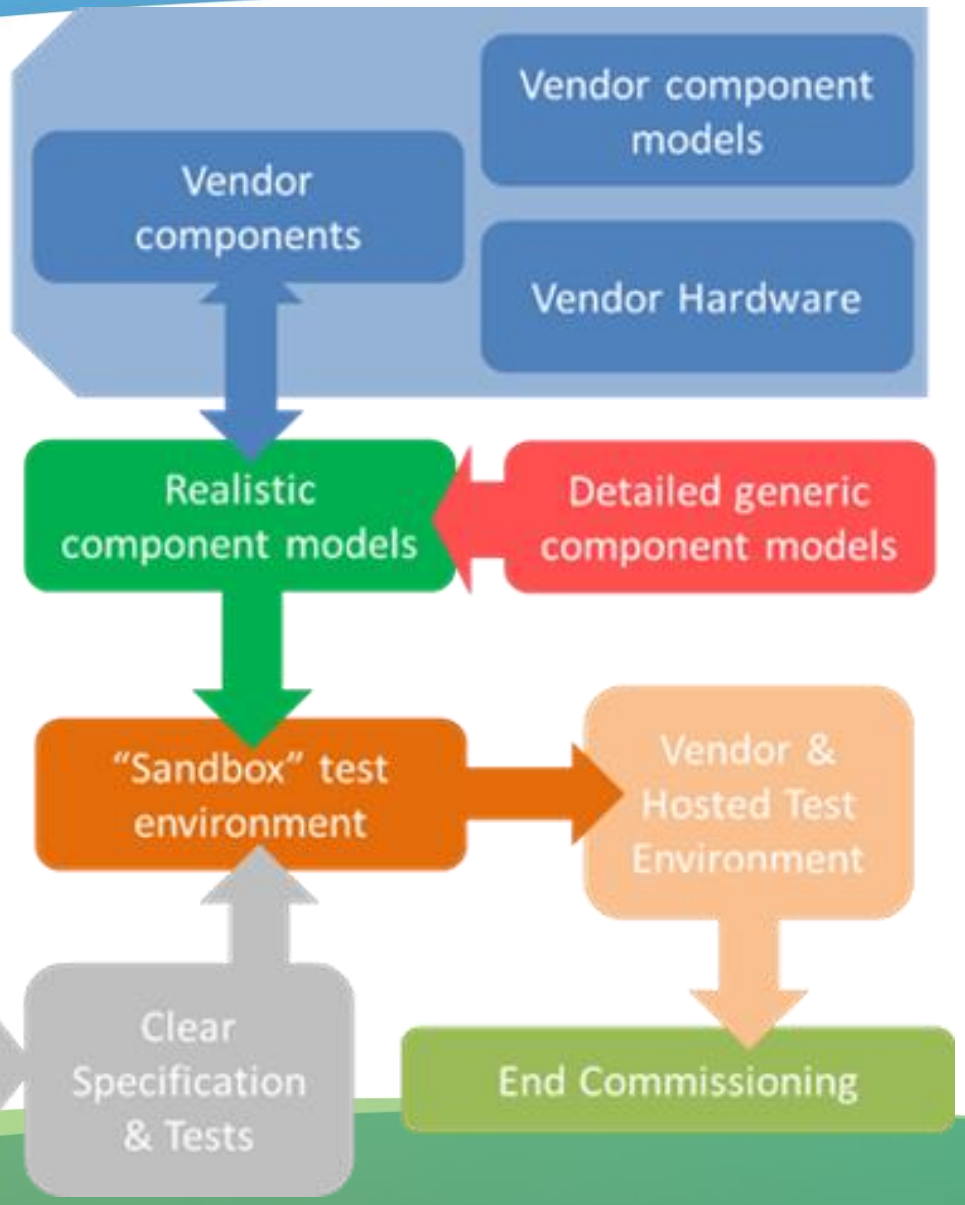
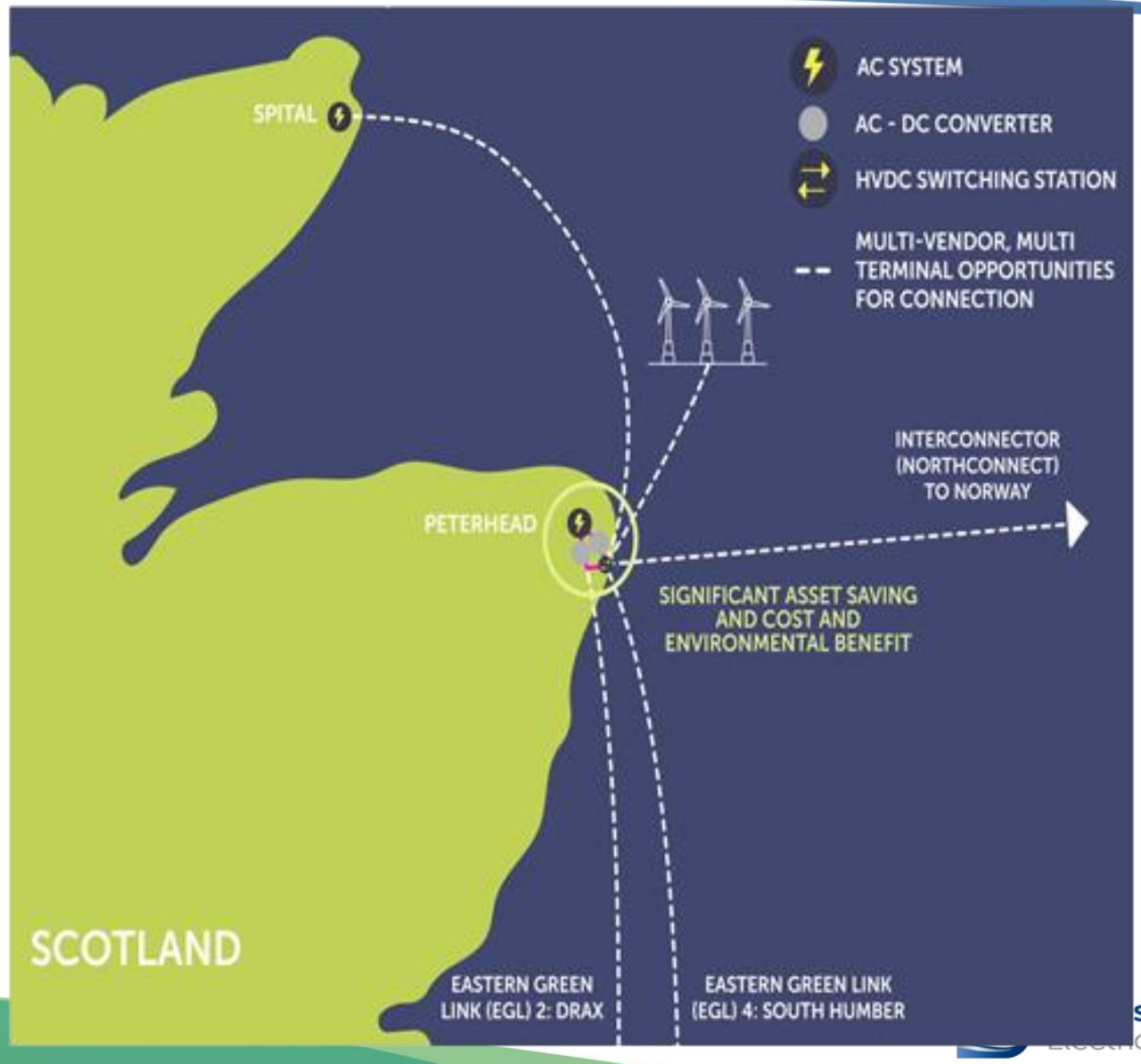
Agenda

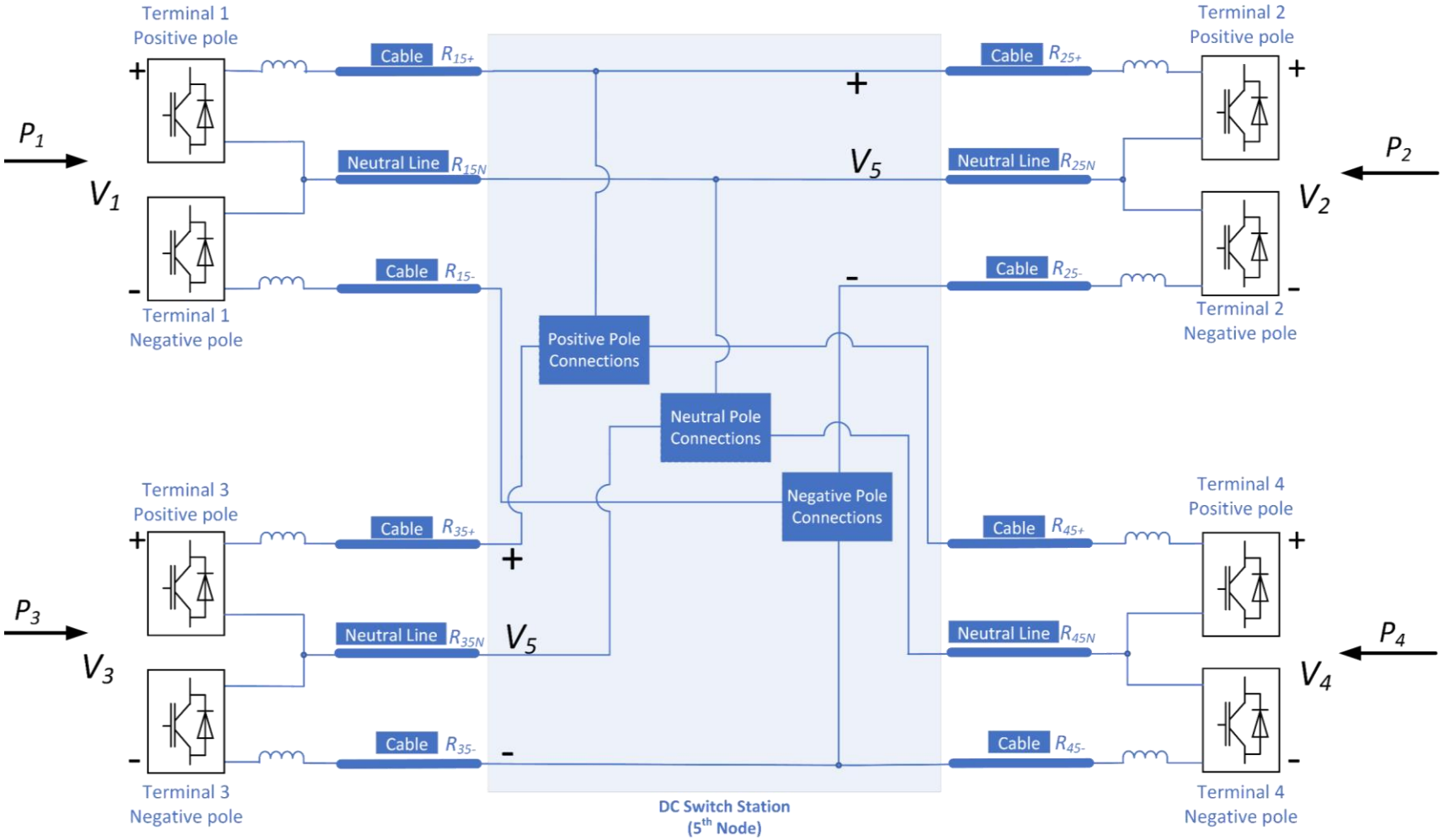
- Recap Context
- Control Architecture
- Specifications to de-risk control interactions
- Demonstration of generic model co-simulated with GE supplied model

Flow Chart before Commissioning Project Aquila





Benchmark System

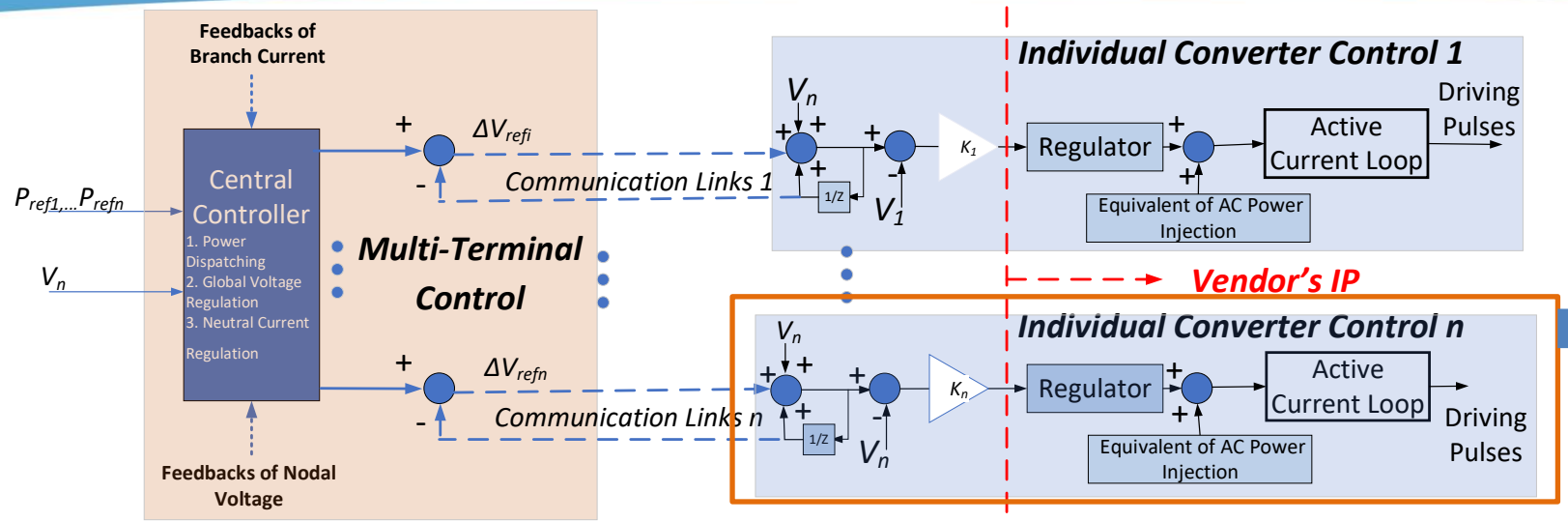


- Radial Network
- Earthing assumptions:
  - Full bipolar terminals unearthed
  - DCSS earthed via low resistance
  - Rigid bipolar terminals earthed via low resistance
- In simulation, the differences between rigid and full bipolar sections are represented by different impedance values of neutral lines
- Control power driven by AC dynamics is future work

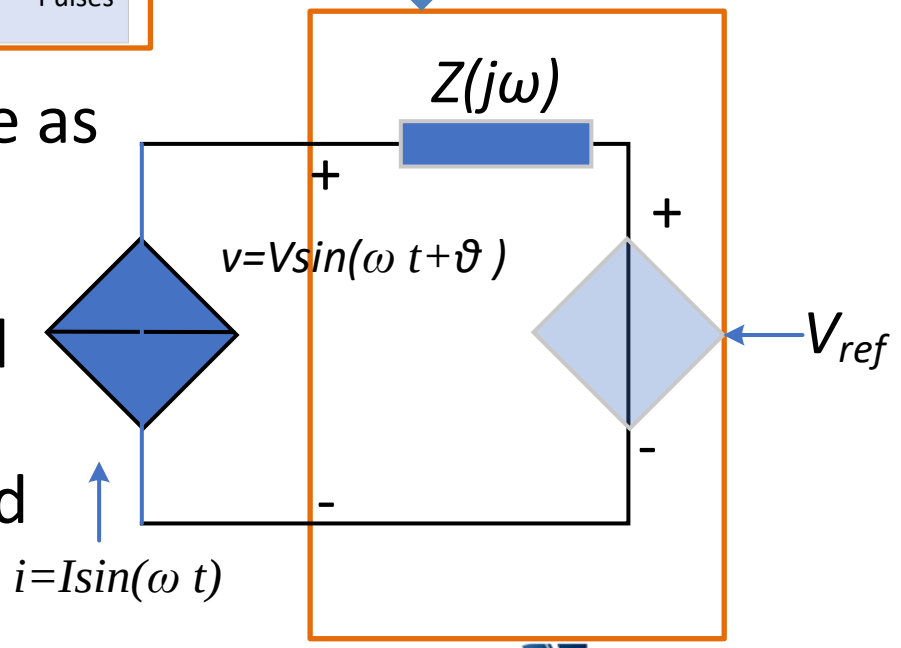
MVMT-HVDC Steady State Control Architecture

- Defining the interfaces of primary control and electrical connection in a vendor agnostic manner
  - performance defined by TSO
  - delivered by vendor
- Secondary control cascaded to the inputs of primary control orders
  - Designed By TSO (HVDC Centre)
  - delivered by vendor
    - ✓ Power control
    - ✓ DC voltage bias control
    - ✓ Neutral Current Control
    - ✓ MIMO optimization functions in future work

What to specify and what to test?



0 - 200 Hz (or more)



- We ask vendor's converter to deliver a performance as a controllable voltage source behind a virtual impedance
- We test the I/O controllability of set values, V_{ref} and $Z(j0)$
- We scan the equivalent impedance $Z(jw)$ over broad frequencies in single converter test

Methodologies to Quantify MVMT-HVDC stability

The National HVDC Centre

- 1.Security domain of power flow
  - "CX-Index" as a global scaler index
  - How "far" an operating point is from the completion of no-load energization
- 2. Small-signal MIMO non-minimum-phase stability over broad frequencies
  - Interaction stability
  - Transfer stability
  - Local stability
- Additional one: robustness against measurement error

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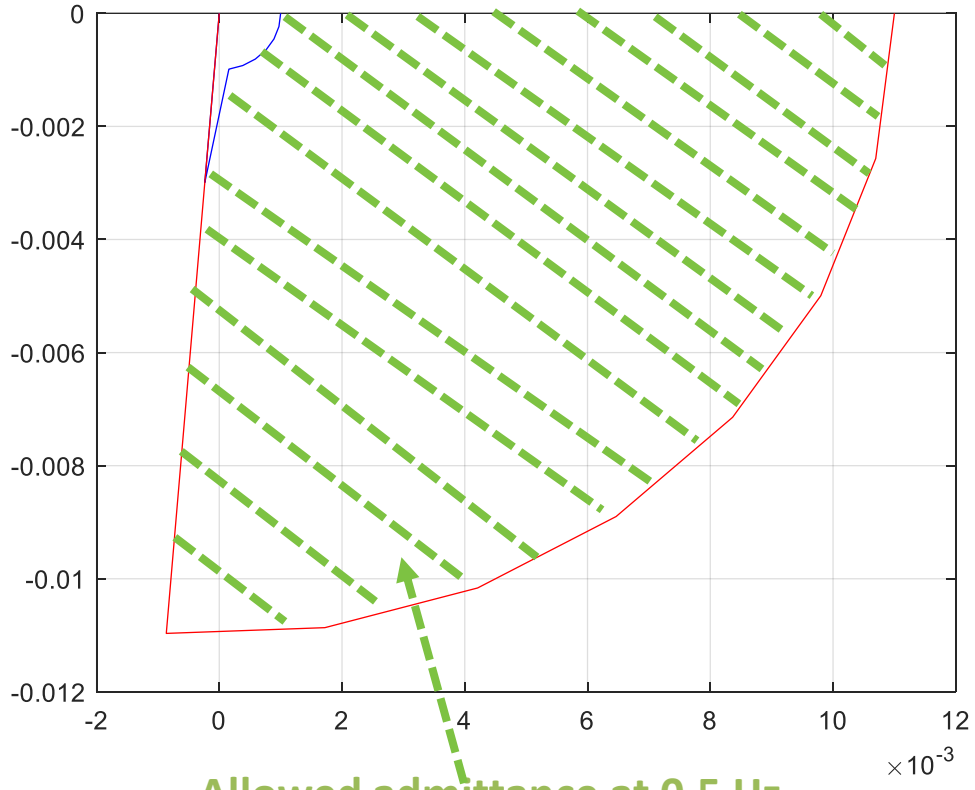
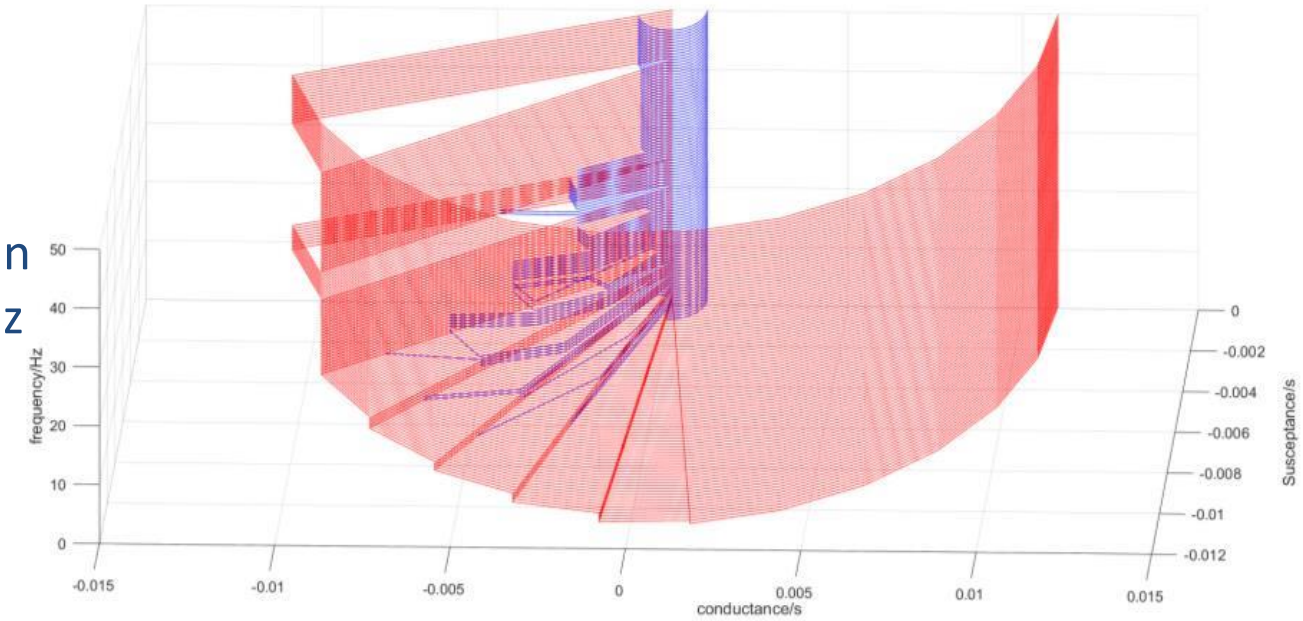
Dummy Specifications for Interaction Stability

- Envelopes of frequency-dependent admittance (I/V) of converter
- Solver Input: Network Impedance → Solve Output: Envelopes of Converter Impedance



Allowed admittance at 0.5 Hz

Solve the envelopes in every 0.5 Hz



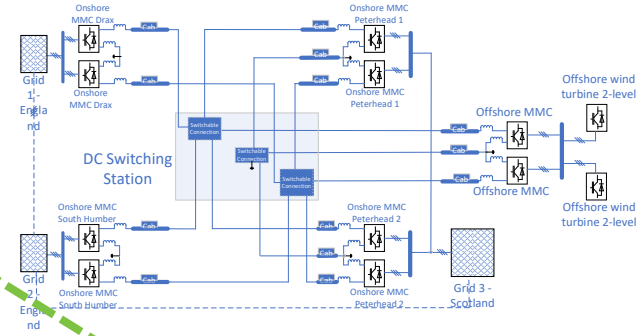
Envelope of admittance up to 50 Hz (or more)

MVMT-HVDC Test Scheme

The National HVDC Centre

Modelling

Upload



We are here now

Operate

Monitor and Analysis

Computing the model for 100,000 ~1000,000 times per second…

Swap generic model with vendor supplied black-boxes in real-time co-simulation

4 principle HVDC Converter Vendors

Verify

Terminal Measurement based offline assessment

Informing technical specifications of MVMT-HVDC (Aquila) project

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